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ORRICK, HERRINGTON & SUTCLIFFE, LLP
4 PARK PLAZA
SUITE 1600
IRVINE, CA 92614-2558

EXAMINER	
CHAUDRY, MUJTABA M	

ART UNIT	PAPER NUMBER
2133	8

DATE MAILED: 01/30/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/768,121	DISTLER ET AL.	
	Examiner	Art Unit	
	Mujtaba K Chaudry	2133	

-- The MAILING DATE of this communication appears on th cover sh et with th correspond nc address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *10 November 2003*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-20* is/are pending in the application.

4a) Of the above claim(s) *21-24* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-20* is/are rejected.

7)☒ Claim(s) *5,14,15 and 17* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *08 May 2001* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. §§ 119 and 120

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

13)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application) since a specific reference was included in the first sentence of the specification or in an Application Data Sheet. 37 CFR 1.78.

a) ☐ The translation of the foreign language provisional application has been received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121 since a specific reference was included in the first sentence of the specification or in an Application Data Sheet. 37 CFR 1.78.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ .
4) ☒ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

Note of Reference

The Applicants are hereby requested to direct all correspondence to the examiner undersigned, as the previous examiner assigned to this case is no longer responsible for this case.

Response to Amendment

Applicant's arguments/amendments with respect to amended claims 4, 6, 18, 20 and 23 and originally filed claims 1-3, 5, 7-17, 19, 21-22 and 24 filed November 10, 2003 have been fully considered and therefore a new grounds of rejection is set forth below.

Election/Restrictions

Restriction to one of the following invention is required under 35 USC 121.

1. Claims 1-20 are drawn to generating test patterns.
2. Claims 21-24 are drawn to test logic circuits.

Applicants' election of claims 1-20 without traverse is acknowledged and therefore claims 21-24 are withdrawn from examination. Applicants' are reminded to cancel non-elected claims 21-24 in next communication. See attached interview summary.

Claim Objections

Claim 5 is objected to because of the following informalities:

- In lines 3-4 the phrase "**...said differential vector data set with attached header form...**" needs to be replaced with "**...said differential vector data set attached with header forms**..."

Claim 14 is objected to because of the following informalities:

- In line 5, the "," after "set" needs to be omitted.

Appropriate correction is required.

Claim 15 is objected to because of the following informalities:

- The term "program" in **"A program storage device..."** is not clear. It should probably be **"A programmable storage device..."** which would make sense.
- In line 3, "a" needs to be inserted before "original test vector data."

Claim 17 is objected to because of the following informalities:

- The preamble of the claim is not sufficient since it does not state for what the method is for. Applicants are advised to state what the method is for in the preamble language.

Claim Rejections - 35 USC § 112

The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

Claim 1 is rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention. The term "highly" in lines 4 and 6 of claim 1 and throughout various claims is not a positive limitation. In other words, "highly" is a relative term and cannot be given patentable weight. Applicants are advised to omit such language.

Claim 4 is rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention. The term "approximately" in line 2 is a relative term and cannot be given patentable weight. Applicants are advised to omit such language.

Claim 13 recites the limitation "...said instructions..." in lines 1-2. There is insufficient antecedent basis for this limitation in the claim. The Examiner suggests to replace, "said instructions" to "said computer-executable instructions." The Examiner presumes the latter for examination purposes.

Claim 15 is rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention. The term "tangibly" in line 1 is a relative term and cannot be given patentable weight. Applicants are advised to omit such language. Furthermore, claim language, in particular of lines 3-4, is unclear. It states, "...by repeating a care bit value encountered in a first test vector of said original test vector in non-care bits of neighboring test vectors." Examiner is not sure what the Applicants wish to convey, since the there is not first test vector in the original test vector. Clarification and/or amendment to the claim language is requested.

Claim 20 is rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the

invention. The term "approximately" in line 2 is a relative term and cannot be given patentable weight. Applicants are advised to omit such language.

Appropriate correction is required.

Claim Rejections - 35 USC § 103

The factual inquiries set forth in *Graham* **v.** *John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.
4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

Claims 1-20 are rejected under 35 U.S.C. 103(a) as being unpatentable over Rajski et al. (USPN 6327687 B1) further in view of Rohrbaugh et al. (USPN 6067651).

As per claims 1, 9, 13, 15 and 17, Rajski et al. (herein after: Rajski) substantially teaches (title and abstract) a method for compressing test patterns to be applied to scan chains in a circuit under test. The method includes generating symbolic expressions that are associated with scan cells within the scan chains. The symbolic expressions are created by assigning variables to bits on external input channels supplied to the circuit under test. Using symbolic simulation, the variables are applied to a de-compressor to obtain the symbolic expressions. A test cube is created using a deterministic pattern that assigns values to the scan cells to test faults within the integrated circuit. A set of equations is formulated by equating the assigned values in the test cube to the symbolic expressions associated with the corresponding

scan cell. The equations are solved to obtain the compressed test pattern. Furthermore, Rajski teaches (col. 5, lines 3-32) that **the remaining scan cells in the test cube may be left unassigned and are filled with a pseudo-random pattern generated by the decompressor during testing. Thus, the ATPG tool generates test vectors without filling the "don't care" positions with random patterns.** The Examiner would like to point out that the test pattern generator does not necessarily fill the don't cares with pseudo-random. Symbolic expressions are generated that are associated with the scan cells and that are a function of externally applied input variables. A set of equations is formulated by equating the symbolic expressions to the values assigned to the scan cells. Solving a set of equations creates the compressed pattern. To generate the symbolic expressions, input variables are assigned to bits applied to the input channels. Symbolic simulation of the decompressor is used to create the symbolic expressions as a linear combination of the input variables. The symbolic expressions are then assigned to the scan cells within the scan chains. After solving the equations, new equations can be incrementally appended to the existing set of equations to test another fault. The resulting new set of equations may be solved if a solution exists. If no solution exists, the most recently appended equations are deleted and another fault is selected. The process of incrementally appending equations by selecting new faults continues until a limiting criteria is reached, such as a predetermined limit of unsuccessful attempts is reached, or a predetermined number of bits in the test cube are assigned values. Rajski teaches a method comprising all the elements of the instant application. Rajski teaches forming a compressed test data by setting a care bits and non-care bits in Figure 8. Rajski et al. teaches a downloading a test data into a testing system and loading input latches in column 4 lines 57-60: "The compressed test pattern is stored in an

ATE and is applied on input channels to an integrated circuit being tested." Rajski teaches decompressing the compressed test vector data (decompressor, 36) in Figure 2. Rajski teaches a computer-usable medium storing computer-executable instructions volume in the testing of logic products comprising all the steps of the instant application. Rajski et al. teaches generating an original test vector in column 5, lines 6-7, which state: "the ATPG tool generates test vectors". Rajski et al. teaches filling non-care bits with a repeated value to form a highly compressible test vector data set in column 8, lines 57-60: "The remaining scan cells that are `don't cares'... in the compressed test pattern and are filled with a pseudo-random values generated" (filling non-care bits with a repeated value to form a highly compressible test vector data set). Rajski et al. teaches compressing the test vector data set to form compressed test vector in column 4, lines 55-57: "A method ... is used to generate a compressed test pattern". Rajski et al. teaches a method for reducing test data volume in the testing of logic products comprising all the steps of the instant application. Rajski et al. teaches generating redundant test vectors in column 5, lines 6-7, which states: "the ATPG tool generates test vectors". Rajski et al. teaches utilizing a repeat capability of a tester to load input latches of the tester in column 4, lines 57-60. Rajski does not explicitly teach to fill the don't care values in the compressed test vector with repeated values as indicated in the response.

However, Rohrbaugh et al. (herein after: Rohrbaugh) teaches, in an analogous art, (title and abstract) a method and apparatus for generating a compacted set of test sequences for use by a tester that tests an integrated circuit having a scan register containing a plurality of bits that define test inputs for the integrated circuit. The method begins by defining a list of faults for the integrated circuit and generates a first test sequence that defines values for those inputs

necessary to detect a target fault selected from the list of faults. The method then adds the first test sequence to a list of test sequences and marks the selected fault as detected. The method then generates an additional test sequence that defines values for those inputs necessary to detect a target fault selected from the list of faults, a fault other than one previously marked as detected. Finally, the preferred method determines whether the additional test sequence may be compacted with any test sequence in the list of test sequences, and if so, compacts the additional test sequence with a test sequence in the set of test sequences. If the additional test sequence may not be compacted with any test sequence in the list of test sequences, the method adds the additional test sequence to the set of test sequences. The process of generating additional test sequences and compacting them, when possible, to sequences in the set of sequences is repeated until a compacted condition is reached. In particular, Rohrbaugh teaches (col. 2, lines 53-65) dynamic compaction operates to generate compacted vectors one at a time. More specifically, a first test vector is generated to test for a given fault in a list of faults to be tested. However, before generating a second test vector, an attempt is made to utilize the first test vector to test for additional faults. In this regard, **the unused bit positions (i.e., don't care values) may be set to either "1"s or "0"s**, or existing bit positions may be utilized, to the extent that the values need not be changed. The Examiner would like to point out that Rohrbaugh teaches setting the don't cares to a repeated value. Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to modified the test vector compaction teachings of Rajski by utilizing the techniques of Rohrbaugh by filling in the don't cares of the test data with a repeated pattern as suggested by Rohrbaugh. One of ordinary skill in the art would have been motivated to modify the test compaction technique of Rajski because by using repeated values

for the don't cares allows convenient demarcation of the care bits from don't care bits and therefore increases the efficiency of testing the integrated circuit.

As per claim 2, Rajski teaches (col. 4, lines 55-68) transmitting the compressed test data to a test system and acquiring the compressed care bits for testing the integrated circuit.

As per claims 3 and 18, Rajski et al. teaches generating a background vector data set (generate a test cube, 62) in Figure 5. Rajski et al. teaches forming a differential vector data set by XORing care bits with background vector bits in Figure 7.

As per claims 4 and 20, Rajski et al. teaches XORing sets a substantial portion of the care bits to a value 0 in Table 8(column 13, lines 44-59).

As per claim 5, Rajski et al. teaches an algorithm (Gauss-Jordan elimination) used in header identification and a seed used to generate vector data in column 10, line 65 through column 11, line 20: " Gauss-Jordan techniques ...It can be verified... resulting seed variables".

As per claim 6, Rajski et al. teaches decompressing the compressed test vector data (decompressor, 36) in Figure 2. Rajski et al. teaches extracting and reconstructing vector data in Figure 4. Rajski teaches XORing the reconstructed background vector data to form a reconstructed test vector data in Figure 7.

As per claims 7 and 10, Rajski et al. teaches reconstructed test data vectors with care bits and non-care bits in Figure 8.

As per claims 8 and 19, Rajski et al. teaches a random distribution of bits having both "0" and "1" in column 3,lines 10-11: "Weighted random patterns have been primarily used".

As per claims 11, 12 and 16, Rajski et al. teaches a test vector data that comprises a matrix of test vectors arranged in rows and columns in Table 2(column 10, lines 46-56). Rajski et al. teaches a different care bit is repeated in the same column for each row of the matrix in Table 4(column 11, lines 24-34).

As per claim 14, Rajski teaches a computer-usable medium storing computer-executable instructions volume in the testing of logic products comprising all the steps of the instant application. Rajski et al. teaches transmitting the compressed test data to a test system and recovering the care bits for loading into input latches of a tester in column 4 lines 57-60.

The Examiner disagrees with the Applicants rejects pending claims 1-20. All arguments have been considered. It is the Examiner's conclusion that amended claims 4, 6, 18, 20 and 23 and originally filed claims 1-3, 5, 7-17, 19, 20 are not patentably distinct or non-obvious over the prior art of record. Furthermore, claims 21-24 are no longer considered for patentability, due to non-election. See election/restriction above.

Conclusion

The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. Rajski teaches a method for compressing test patterns to be applied to scan chains in a circuit under test. , Rohrbaugh teaches a method and apparatus for generating a compacted set of test sequences for use by a tester that tests an integrated circuit having a scan register containing a plurality of bits that define test inputs for the integrated circuit. The Examiner

would like to point out that the Rajski patent is not included in the cited references since in was used in a previous rejection and Applicants should already have it.

Any inquiries concerning this communication should be directed to the examiner, Mujtaba Chaudry who may be reached at 703-305-7755. The examiner may normally be reached Mon – Thur 7:30 am to 4:30 pm and every other Fri 8:00 am to 4:00 pm.

If attempts to reach the examiner by telephone are unsuccessful, please contact the examiner's supervisor, Albert DeCady at 703-305-9595. The fax phone number for the organization where this application is assigned is 703-746-7239.

Any inquiry of general nature or relating to the status of this application or proceeding should be directed to the receptionist at 703-305-3900.

Mujtaba Chaudry
Art Unit 2133
January 13, 2004

ALBERT DECADY
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2100